

METHOD AND DEVICE FOR MANUFACTURING BONDING PADS FOR CHIP SCALE PACKAGING

ABSTRACT OF THE DISCLOSURE

An integrated circuit chip and method of manufacture. The chip has a
5 substrate, e.g., silicon, silicon on insulator, epitaxial wafer. The substrate has a plurality of
chip structures. A plurality of bonding pads are disposed on the substrate. Each of the
bonding pads is formed from an aluminum bearing material or other like material. A surface
region is formed on each of the bonding pads. An under bump metal layer ("UBM") is
overlying the surface region. A wetting layer is formed overlying the under bump metal
10 layer. The wetting layer comprises a plurality of protrusions extending out of the wetting
layer and disposed spatially on the wetting layer. A bump layer is formed overlying the
wetting layer and is mechanically coupling to the plurality of protrusions.

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